TELEDYNE LECROY
Everywhereyoulook™

Summit™ T3-16 Analyzer
for PCI Express® 3.0

Key Features

- **Find errors fast**
  - One button error check
  - Fast upload speed
  - Large trace memory
  - Powerful triggering/filtering
- **See and understand the traffic**
  - Get useful information
  - More choices of data views
  - More ways to analyze data
  - Verification Script Engine included
- **Accurate data capture**
  - 100% data capture at 8 GT/s on all lane widths up to x16
- **Most Extensive Probing Accessories in the PCIe Protocol Test Industry**
  - Backward compatible with existing Teledyne LeCroy Gen1 and Gen2 PCI Express probes

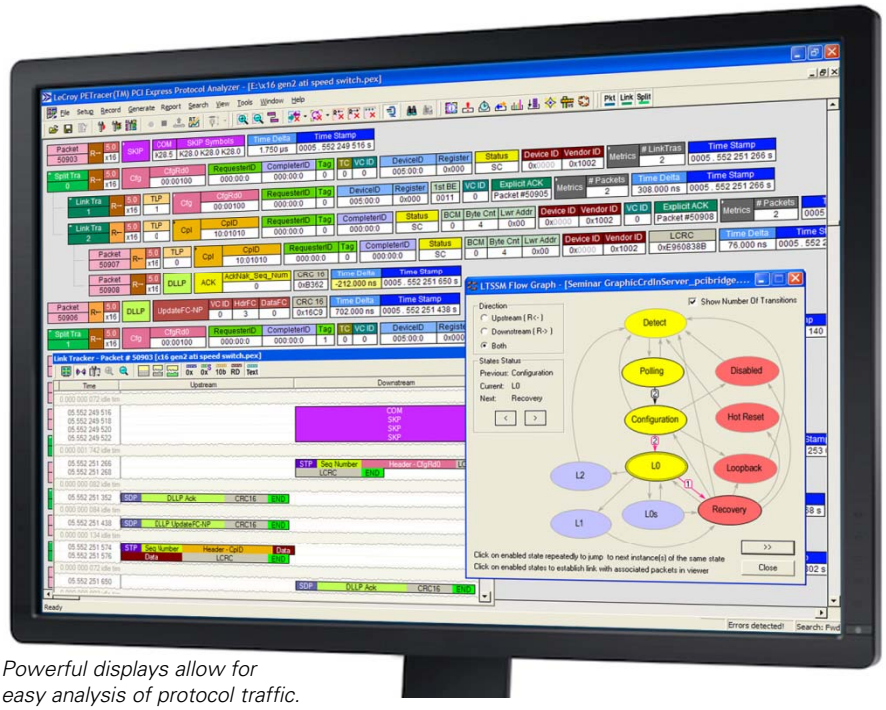
The Summit T3-16 is Teledyne LeCroy's highest performance PCI Express analyzer, and offers advanced features such as: support for PCI Express Spec 3.0; data rates of 2.5 GT/s, 5 GT/s and 8 GT/s; full data capture on bidirectional lane widths of x1, x2, x4, x8 and x16; and 8 GB of trace memory. The product is ideal for high-performance protocol development for add-in boards, servers and workstations, and for customers currently working on PCIe 1.0 and 2.0 applications but with PCIe 3.0 on their roadmaps.

The Summit T3-16 Protocol Analyzer is a high-end analyzer that offers new features for Gen3 application development. While sharing application compatibility with the previous analyzer platforms, the Summit can record traces on SSC supported lanes at speeds of 2.5, 5 and 8 GT/s. Users acquainted with Teledyne LeCroy's multiple probing accessories will find the right probing required to do the job.

The demands of debugging Gen3 speeds require new capability to reduce debugging time and accelerate time-to-market. The auto sense link feature allows tracing of the complete negotiation sequence for both link width and link speed. Lane swizzling allows maximum flexibility to accommodate specialized or unique board layouts for MidBus connections. All events on links can be analyzed in both upstream and downstream directions.

The BitTracer™ software option records the bytes exactly as they come across the link, allowing debugging of PHY layer problems and combining the features of a logic analyzer format with a decoded protocol analyzer format.

The Summit T3-16 for PCI Express utilizes the CATC Trace™ to assist users in analyzing how PCI Express components work together in diagnosing problems. The interface helps find errors fast by using the powerful triggering, filtering and error reporting. View meaningful reports about performance and protocol behavior in real time, and post captured traffic. The CATC Trace is a powerful and intuitive expert software system, embedding detailed knowledge of the protocol hierarchy and intricacies as defined in the protocol specification. The CATC Trace utilizes a graphical display that has been optimized for fast



Powerful displays allow for easy analysis of protocol traffic.

and easy navigation through a captured traffic session. Users are alerted as violations are detected at all levels of the protocol layering, and can easily drill down to areas of interest or collapse and hide fields that are not relevant. Protocol data can be viewed in several ways from logical to chronological, and by events unique to PCI Express.

Know that your data is accurate through reliable and complete decodes of Transaction Layer Packets (TLPs), Data Link Layer Packets (DLLPs), and all primitives for PCI Express for all lane widths. Setting up and taking a trace is simple to do without the worry of extra plugin platforms or complex networking issues.

Features	Benefits
Powerful & Intuitive CATC Trace Expert Software	Faster interpretation and debug of PCI Express traffic.
Extensive Decoding	Understand the protocol completely with accurate and reliable decoding of TLPs (Transaction Layer Packets) and DLLPs (Data Link Layer Packets) and all Primitives for PCI Express.
Advanced Triggering/Filtering	Find Errors fast by isolating important traffic, specific errors or data patterns. Understand transactions more clearly by removing non-essential fields from the trace.
Intelligent Reporting	Quickly identify and track error rates, abnormal link or timing conditions, display configuration space, and protocol specification details.
Dword to Transaction Level Viewer	See and understand Symbol, Packet, Link and Split Transaction levels of the PCI Express protocol.
Monitoring and Link Utilization	Troubleshoot throughput, link utilization, and bandwidth issues.
BitTracer Software Option	Records the bytes as they come across the link. Allows debugging of PHY layer problems. Gives protocol analyzer the best of both worlds; a logic analyzer format and decoded protocol analyzer format.
Auto Sense Link	Analyzes all traffic negotiation between two devices of different lane widths.
Lane Swizzling	Accommodates specialized or unique board layouts for MidBus connections.
Deep Buffer Recording Capacity	Capture long recording sessions for analysis and problem solving up to 8 GB (4 GB in each direction).
I/O Virtualization	Test SR/MR-IOV in the platform context to assure robust virtualization designs.
High-speed Interface Ports	No complicated setup required, with 1 Gb/s Ethernet and USB 2.0 ports available.
Downloadable Trace Viewer	Share and annotate trace recordings within a development team.

Additional Features

- ✓ Protocol Hierarchical Display
- ✓ Dword view
- ✓ Data Flow View
- ✓ Trace Navigator
- ✓ TLP Packet Script Decoding
- ✓ Trigger/Filter Control
- ✓ ZeroTime™ Search
- ✓ Header Field Viewer
- ✓ Config Spec Viewer
- ✓ Advanced Hide
- ✓ Timing Calculator
- ✓ Performance Metrics
- ✓ Flow Control Credit Tracking
- ✓ Automation API
- ✓ Expert Recording Buffer Size
- ✓ Expert Real-time Bus Monitoring
- ✓ Expert Triggering
- ✓ Expert Traffic Summary View
- ✓ Expert Graphical Bus Utilization View
- ✓ Verification Script Engine
- ✓ 1 GB/s Ethernet & USB 2.0

Ordering Information

Product Description	Product Code
Summit T3-16 Gen3 x8 Analyzer	**PE051AAA-X**
Summit T3-16 Gen3 x16 Analyzer	**PE050AAA-X**
Summit T3-16 Gen3 x8 MidBus Probe Kit (two kits required for x16)	**PE050ACA-X**
PCI Express Gen 3 x8 Dish for MidBus Probe (two probes required for x16)	**PE038UIA-X**
Gen3 x16 Interposer	**PE039UIA-X**

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Local sales offices are located throughout the world.
Visit our website to find the most convenient location.

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